Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A method of manufacturing an insulated gate field effect transistor, the method comprising:

providing a substrate having a first major surface having a low-doped region at the first major surface, the low-doped region having a concentration of less than $5x10^{14}$ cm^{-3} at the first major surface;

forming gate trenches extending from the first major surface;

forming trench insulator on a base and sidewalls of the gate trenches;

implanting dopants of a first conductivity type at the base of the trenches;

implanting a body implant of second conductivity type opposite to the first conductivity type in the low-doped regions between the gate trenches;

carrying out a diffusion step to form an insulated gate field effect transistor structure in which the body implant diffuses towards the substrate in the low-doped region to form a p-n junction ~~below~~ above a drain region and between a body region and the drain region, wherein the body region is doped to have the second conductivity type and the drain region is doped to have the first conductivity type, the p-n junction being deeper below the first major surface between the trenches than at the gate trenches; and

forming source regions at the first major surface adjacent to the gate trench.

2. (previously presented) A method according to claim 1 in which the p-n junction boundary between drain and body region is deeper between the gate trenches than the depth of the trenches.

3. (previously presented) A method according claim 1 in which the insulated gate field effect transistor structure formed in the diffusion step has an additionally doped

region of first conductivity type at the base of the gate trenches having a doping density below $5x10^{16}$ cm^{-3} but higher than in the drain regions between the gate trenches.

4. (previously presented) A method according claim 1, wherein implanting the body implant comprises implanting the body implant with a dose of at most $5x10^{13}$ cm^{-2}.

5. (previously presented) A method according to claim 1 further comprising:

forming a pattern laterally across the first major surface of the substrate, the pattern doped to have lower-doped regions of first conductivity type alternating with higher-doped regions of first conductivity type, wherein the lower-doped regions have a concentration of less than about $5x10^{14}$ cm^{-3} and, the higher-doped regions have a concentration between about $1x10^{16}$ cm^{-3} and $3x10^{16}$ cm^{-3};

wherein the gate trenches are formed in the higher-doped regions.

6. (currently amended) A method according to claim 5 wherein forming the pattern laterally across the first major surface of the substrate comprises:

depositing an epilayer of semiconductor doped to have a doping density lower than a doping density of a trench;

patterning a plurality of trench ~~etch~~ windows spaced laterally across the substrate; and

implanting dopants though the trench ~~etch~~ windows, the dopants being of a first conductivity type;

wherein forming the gate trenches in the higher-doped regions comprises etching gate trenches through the trench ~~etch~~ windows.

7. (previously presented) A method according to claim 5 wherein forming the pattern laterally across the first major surface of the substrate comprises:

etching a plurality of semiconductor trenches spaced laterally across the substrate in a layer of doping density lower than a doping density of the semiconductor trenches; and

growing semiconductor doped to have a doping density in the semiconductor trenches higher than the doping density of the layer of the substrate.

8. (previously presented) A method according to claim 7, wherein the semiconductor is silicon and the first conductivity type is n-type.

9. (currently amended) A method according to claim 1, for making an insulating gate field effect transistor of predetermined breakdown voltage for which the doping of an epilayer for forming an insulated gate field effect transistor without the step of implanting dopant at ~~the~~ a gate of the gate trench has a first predetermined doping concentration;

wherein the doping of the low-doped region at the first major surface is at most one half of the predetermined doping concentration.

10. (previously presented) A method according to claim 1, further comprising performing a moat etch by etching the first major surface to form the gate trenches to a depth below the bottom of the source region.

11. (canceled)